PCB Layout and Design Considerations for the CH7308 SDVO LVDS Transmitter

1. Introduction

This application note focuses on the basic PCB layout and design guidelines for the CH7308 LVDS Output Device with SDVO inputs. SDVO is a digital video interface developed by Intel. Guidelines in component placement, power supply decoupling, grounding, input signal interface and video components for the LVDS interface are discussed in this document. The guidelines discussed here are intended to optimize the PCB layout and applications for this product. They are only for reference. Designers are urged to implement the configurations and evaluate the performance of the system prior to bringing the design to production.

The discussion and figures that follow reflect and describe connections based on the 64-pin LQFP package of the CH7308. Please refer to the CH7308 datasheet for the details of the pin assignments. See **Table 1** for the maximum supported pixel rates for both versions of the CH7308. For the CH7308B, the HSWidth must be set to an even value in the Detailed Timing Descriptor (DTD). The DTD can be modified using the Intel BMP program. The required external circuits and connectivity of the CH7308A and the CH7308B are identical. All the Figures in this Application Note are based off of the CH7308A. The CH7308B is to be connected in the same fashion.

Table 1: Maximum Supported Pixel Rates

Device	Single Channel LVDS	Dual Channel LVDS
CH7308A	140MP/s	100MP/s - 140MP/s
CH7308B	165MP/s	100MP/s - 165MP/s

2. Component Placement and Design Considerations

Components associated with the CH7308 should be placed as close as possible to the respective pins. The following discussion will describe guidelines on how to connect critical pins, as well as describe the guidelines for the placement and layout of components associated with these pins.

2.1 Power Supply Decoupling

The optimum power supply decoupling is accomplished by placing a 0.1µF ceramic capacitor to each of the power supply pins as shown in **Figure 1**. These capacitors (C1, C2, C5, C6, C7, C8, C9, C10 and C13) should be connected as close as possible to their respective power and ground pins using short and wide traces to minimize lead inductance. Whenever possible, a physical connecting trace should connect the ground pins of the decoupling capacitors to the CH7308 ground pins, in addition to ground vias.

2.1.1 Ground Pins

The analog and digital grounds of the CH7308 should connect to a common ground plane to provide a low impedance return path for the supply currents. Whenever possible, each of the CH7308 ground pins should connect directly to its respective decoupling capacitor ground lead, then connected to the ground plane through a ground via. Short and wide traces should be used to minimize the lead inductance. See **Table 2** for the Ground pins assignment.

2.1.2 Power Supply Pins

Separate Digital, LVDS, Analog, and LVDS PLL power planes are recommended. See **Table 2** for the Power supply pins assignment.

Table 2: Power Supply Pins Assignment of the CH7308

Pin Assignment	# of Pins	Type	Symbol	Description
16, 49	2	Power	DVDD	**Digital Supply Voltage (2.5V)**
13, 31	2	Power	DGND	**Digital Ground**
19, 25, 38, 44	4	Power	LVDD	**LVDS Supply Voltage (3.3V)**
22, 28, 35, 41	4	Power	LGND	**LVDS Ground**
56, 62	2	Power	AVDD	**Analog Supply Voltage (2.5V)**
53, 59	2	Power	AGND	**Analog Ground**
3	1	Power	AVDD_PLL	**LVDS PLL Supply Voltage (3.3V)**
8	1	Power	AGND_PLL	**LVDS PLL Ground**

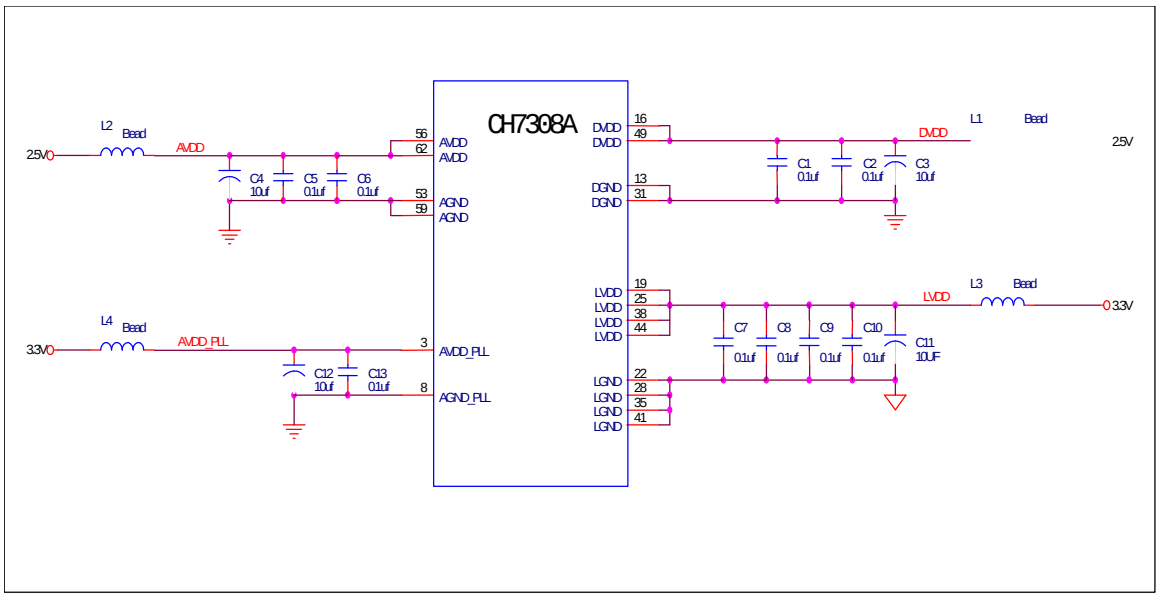

Figure 1: Power Supply Decoupling and Distribution

Notes: All the Ferrite Beads described in this document are recommended to have an impedance of less than 0.05Ω at DC; 23Ω at 25MHz & 47Ω at 100MHz. Please refer to Fair_Rite part# 2743019447 for details or an equivalent part can be used for the diagram.

2.2 General Control and SDVO Signals

- **AS pin**

  The Address Select pin (pin 5) can be configured as shown in **Figure 2**. This pin determines the Device Address Byte of the CH7308. If the AS is pulled 'low', the Device Address for the serial port becomes 72h. If AS is pulled 'high', the serial port Device Address is 70h.

  Note: When using the Intel® driver for the CH7308, the AS pin must be pulled 'high' for a single chip design. For a dual CH7308 design, the AS pin of the primary or default CH7308 should be pulled ‘high’ and the AS pin of the secondary CH7308 should be pulled ‘low’.

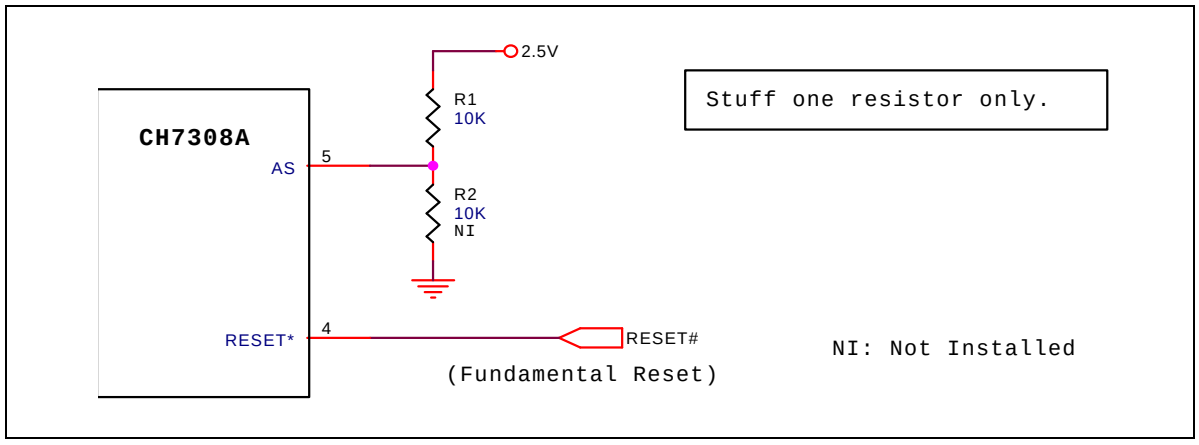

Figure 2: AS pin and RESET* pin connection

- **RESET* pin**

  The RESET pin should be connected to the Fundamental Reset of the GMCH as shown in **Figure 2**. When this pin is pulled 'low', the device is held in the power-on reset condition. When this pin is high, the reset of the device is controlled through the serial port.

- **Serial Video Inputs**

  (SDVO_CLK-, SDVO_CLK+, SDVO_R-, SDVO_R+, SDVO_G-, SDVO_G+, SDVO_B-, SDVO_B+)

  Since the digital serial data of the CH7308 may toggle at speeds up to 2 GHz (depending on input clock speed), it is strongly recommended that the connection of these video signals between the graphics controller and the CH7308 be kept short (maximum 4 inches from edge finger to the CH7308) and be isolated as much as possible from the analog outputs and analog circuitry. For optimum performance, these signals should not overlay the analog power or analog output signals. It is recommended that 5 mil traces be used in routing these signals. There should be 7 mil spacing between each intra pair (e.g. Red+ to Red-). Spacing between inter pairs (e.g. Red to Green) should be 20 mils. The length for a pair of intra differential signals should be matched within 5 mils. The length for inter pairs should be matched within 2 inches. Bends greater than 45 degrees should be avoided. The AC coupling capacitors for the serial video inputs must be placed close to the GMCH.

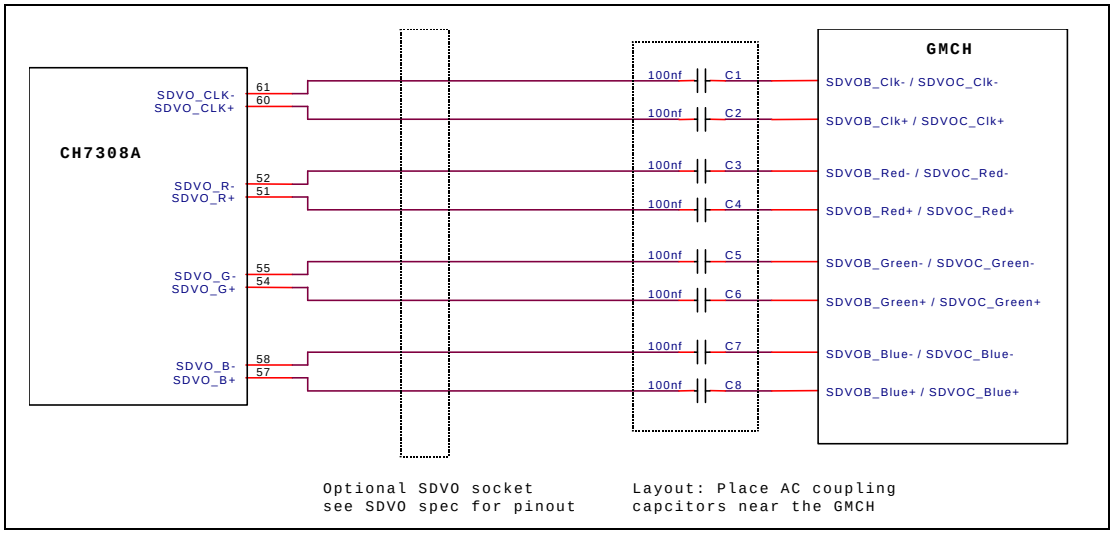

Figure 3: Differential serial video inputs

- **BSCAN**

BSCAN (Pin 63) enables the boundary scan for in-circuit testing. It should be grounded with a 10K resistor in normal operations (See **Figure 4**).

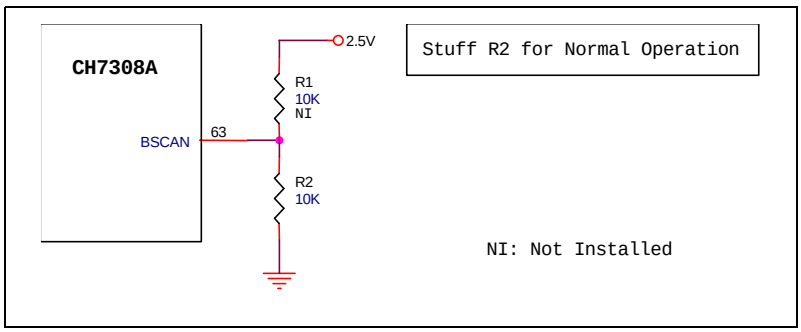

Figure 4: BSCAN strapping options

To enable the boundary scan test function, please follow the procedure described in the latest CH7308 datasheet

2.3 Serial Port Interface

- **SPD and SPC pins**

SPD (pin 7) and SPC (pin 6) function as a serial interface where SPD is bi-directional data and SPC is an input only serial clock. In the reference design, SPD and SPC are pulled up with 5.6 KΩ resistors to 2.5V (See **Figure 5**).

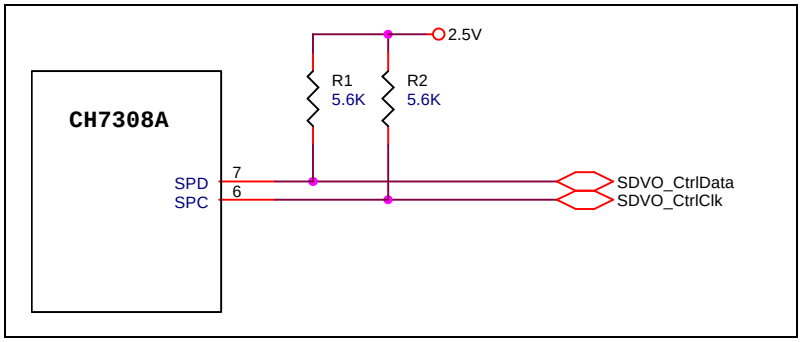

Figure 5: Serial Port Interface: SPD and SPC pins

- **SD_PROM and SC_PROM**

SD_PROM (pin 9) and SC_PROM (pin 10) are used to interface with the serial PROM on the ADD2[1] card. In the reference design, SD_PROM and SC_PROM are pulled up with 5.6 KΩ resistors (See **Figure 6**). If the design is on the motherboard-down, the PROM is not required and both SD_PROM and SC_PROM can be either pulled up or floating.

[1]Note: ADD2 Card: Advanced Digital Display Card - 2nd Generation. It provides digital display options for an Intel® graphics controller that supports the SDVO interface. It will not work with the graphics controller that supports Intel® DVO interface

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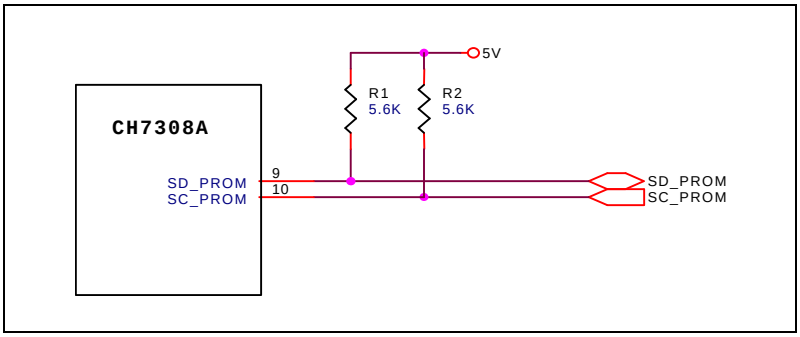

Figure 6: Serial Port Interface: SD_PROM and SC_PROM pins

- **SD_DDC and SC_DDC**

SD_DDC (pin 11) and SC_DDC (pin 12) are used to interface with the DDC receiver. In the reference design, SD_DDC and SC_DDC are pulled up with 5.6 KΩ resistors to 5V (See **Figure 7**). Close attention must be paid close attention to the DDC voltage. Not all DDC interfaces are 5V. In the case where the DDC voltage is 3.3V, R1 and R2 should be changed to 3.3KΩ or 3.6KΩ.

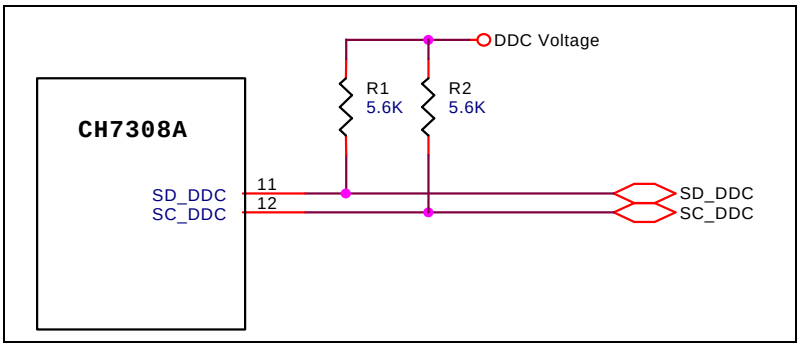

Figure 7: Serial Port Interface: SD_DDC and SC_DDC pins

2.4 CH7308 Design Options

- **Single CH7308 design**

The connection for a single CH7308 design is shown in **Figure 8**. Either SDVO port (SDVOB or SDVOC) can be used. The AS pin, pin 5, should be pulled high. The SPD EEPROM should be connected to this device.

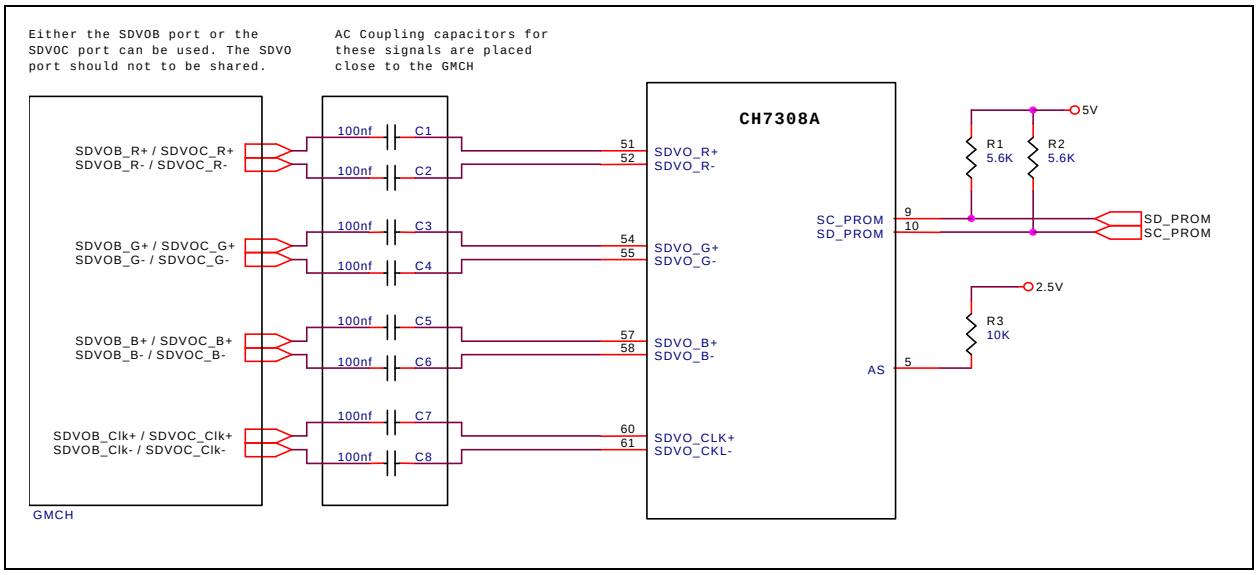

Figure 8: Single CH7308 design

- ## Dual CH7308 design

  The connection for a dual CH7308 design is shown in **Figure 9**. Either SDVO port (SDVOB or SDVOC) can be used for either SDVO LVDS Transmitter. The AS pin, pin 3, should be pulled 'high' for one device and 'low' for the other device. Only one SPD EEPROM is necessary and must be connected to the SDVO DVI Transmitter which has the AS pin pulled 'high'.

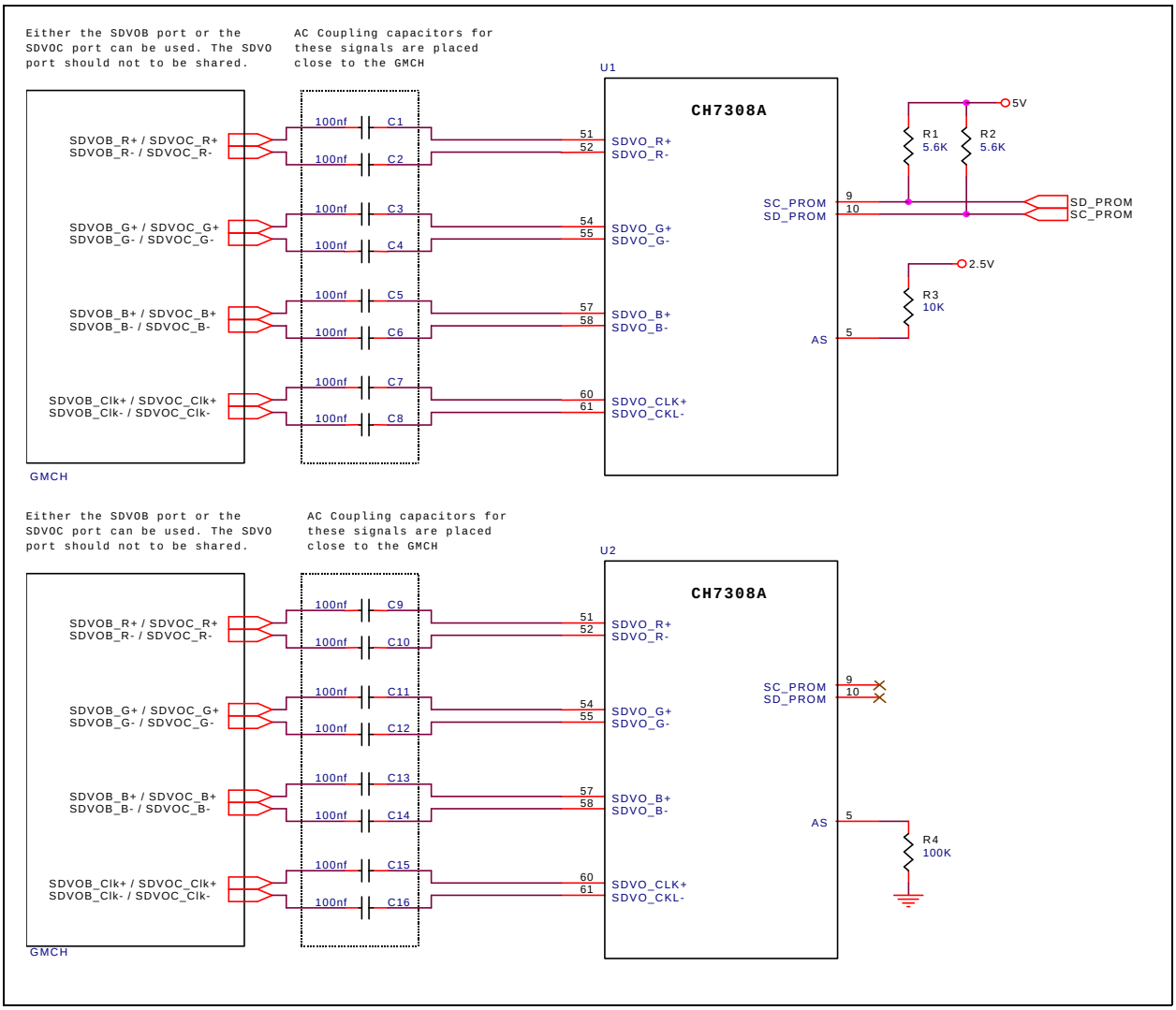

Figure 9: Dual CH7308 design

2.5 LVDS Output and Control

- **VSWING (LVDS Swing Control)**

  This pin (Pin 32) sets the swing level of the LVDS outputs. A 2.4KΩ resistor should be connected between this pin and LGND using short and wide traces (See **Figure 10**).

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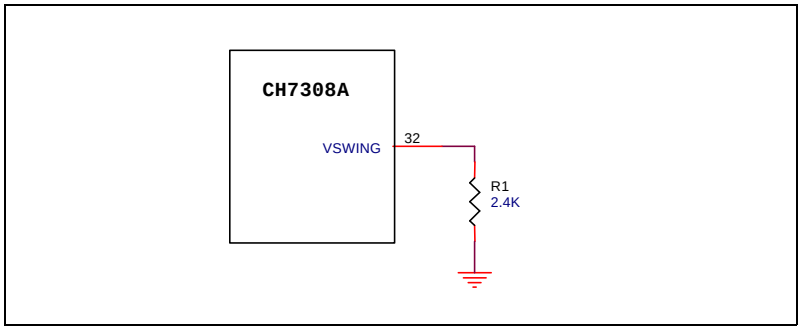


Figure 10: VSWING Connection

- **LVDS Output**

The LVDS in interface is similar to the SDVO interface with respect to speed and the fact that they are both differential interfaces. The following applies to both interfaces:

1. Keep traces as short as possible.

2. Make these traces have a 100 ohm differential impedance.

3. Trace widths should be 5 mils.

4. Intra Pair spacing (spacing between the "+" and "-" pairs) should be 7mils.

5. Inter Pair spacing (spacing between one differential pair and another) should be a minimum of 20 mils.

6. Difference in trace lengths between "+" and "-" pairs should be within 5mils.

7. "+" and "-" pairs should be routed in parallel.

2.6 Important Design Considerations (Panel power, backlight power, and EDID (DDC) pull-up voltage)

- **LVDS Power**

Close attention must be paid to the power supplied to the LVDS backlight and the LVDS panel. Power requirements may differ from panel to panel. Please check the panels power and backlight voltage specifications. ENABKL (pin1) and ENAVDD (pin2) of the CH7308 can be used as control signals to turn on the power to the LVDS backlight and the LVDS logic circuitry.

- **EDID Pull-up**

The voltage of the EDID serial EEPROM varies from panel to panel as well. Communication to the EDID of the LVDS panel is done through the SC_DDC (pin 12) and SD_DDC (pin 11) pins of the CH7308. These pins require a 4K - 9K ohm resistor pulled up to the same voltage as the voltage used for the EDID on the chosen LVDS panel.

3. Reference Design Example

The following schematics are based on an Intel® Grantsdale-G graphics chipset design and are to be used as a CH7308A PCB design example only. It is not a complete design. Those who are seriously doing an application design with the CH7308A and would like to have a complete reference design schematic, should contact Applications within Chrontel, Inc. For SDVO/LVDS designs which require pixel rates over 140MP/s, the CH7308A can be substituted with the CH7308B in the following schematics..

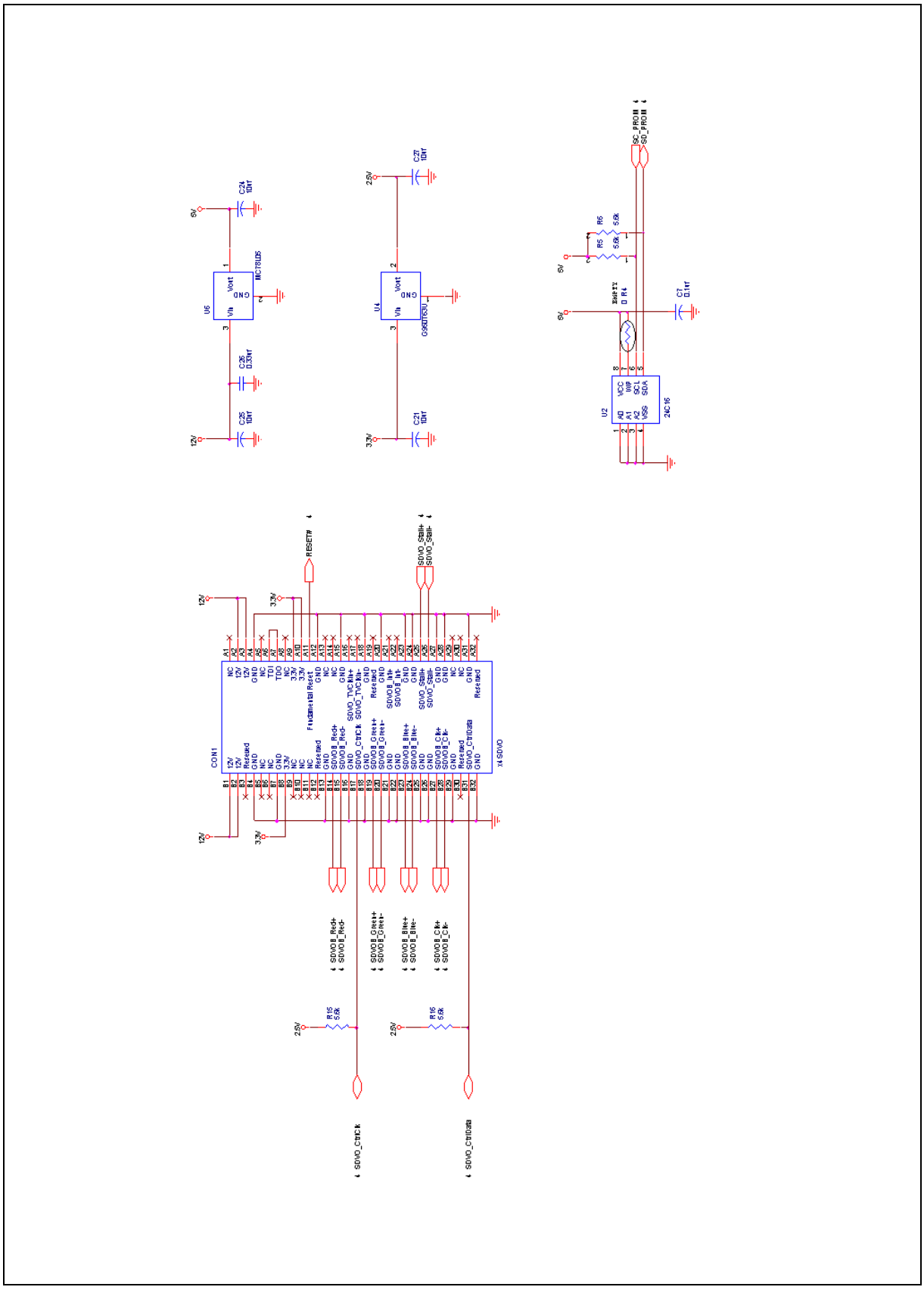
3.1 Schematics of Reference Design Example

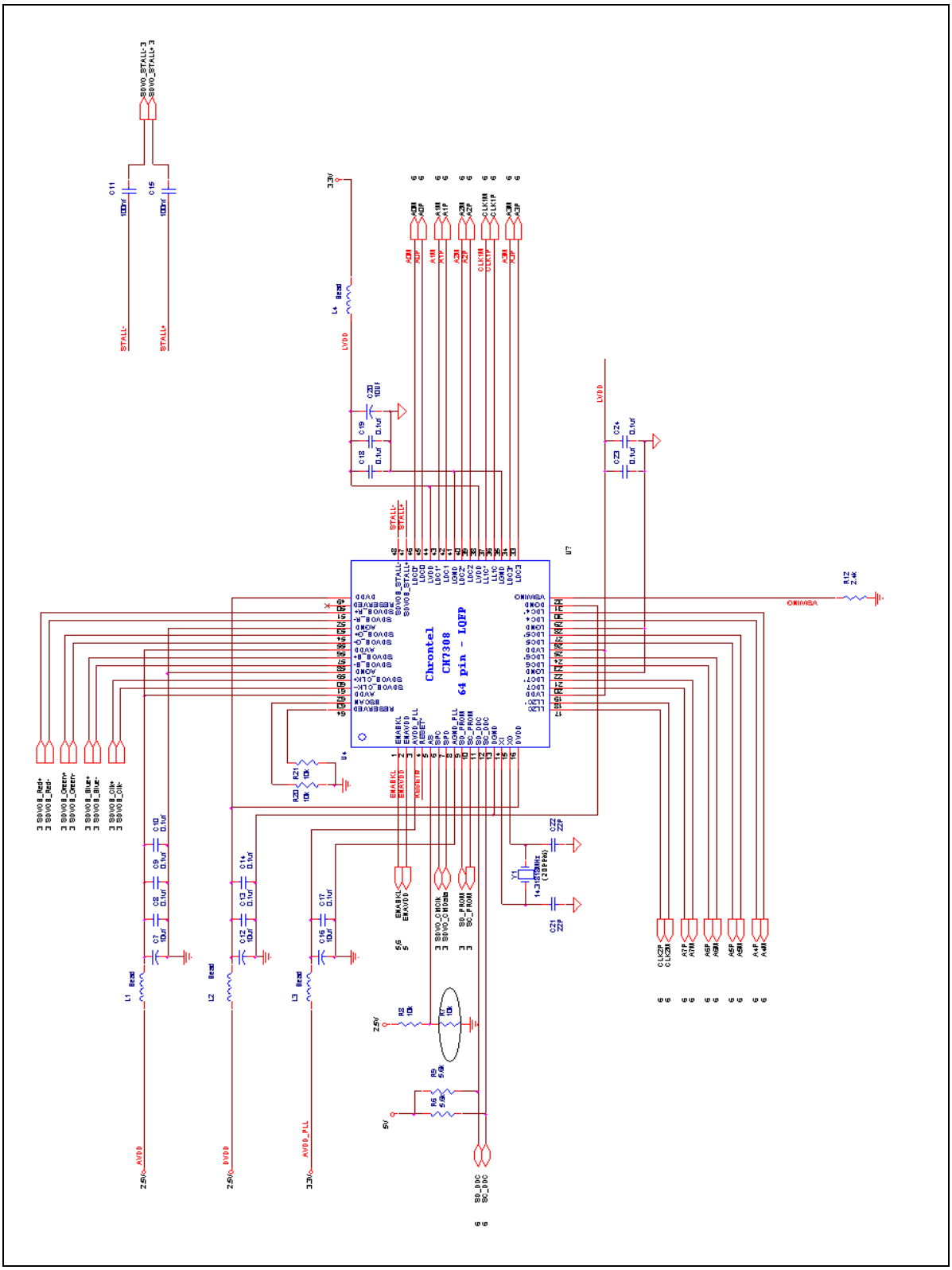
Assembly Instructions:

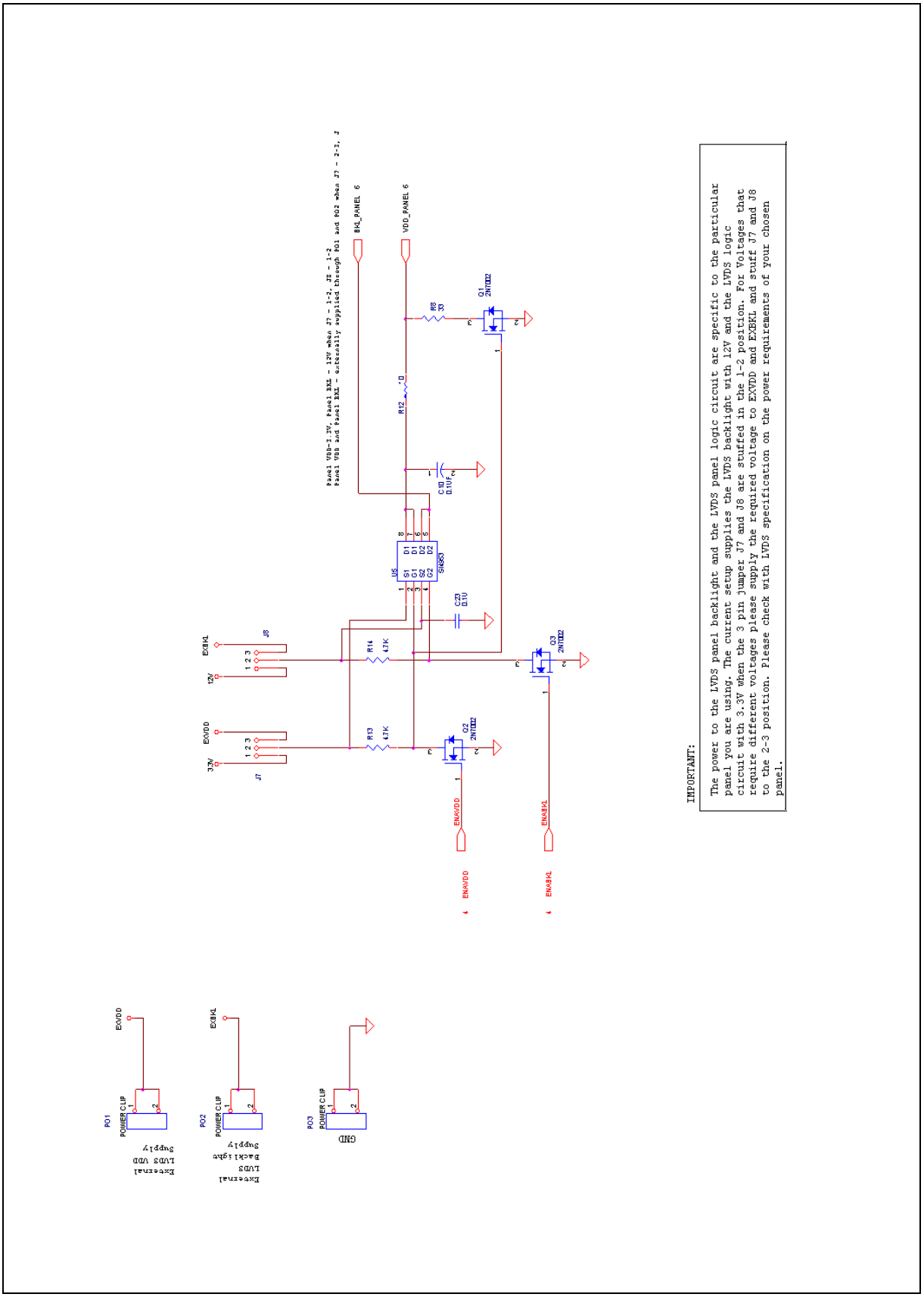
Note: Contents within the "ellipse" are NOT STUFFED! It is used only as options.

Do not stuff following items :

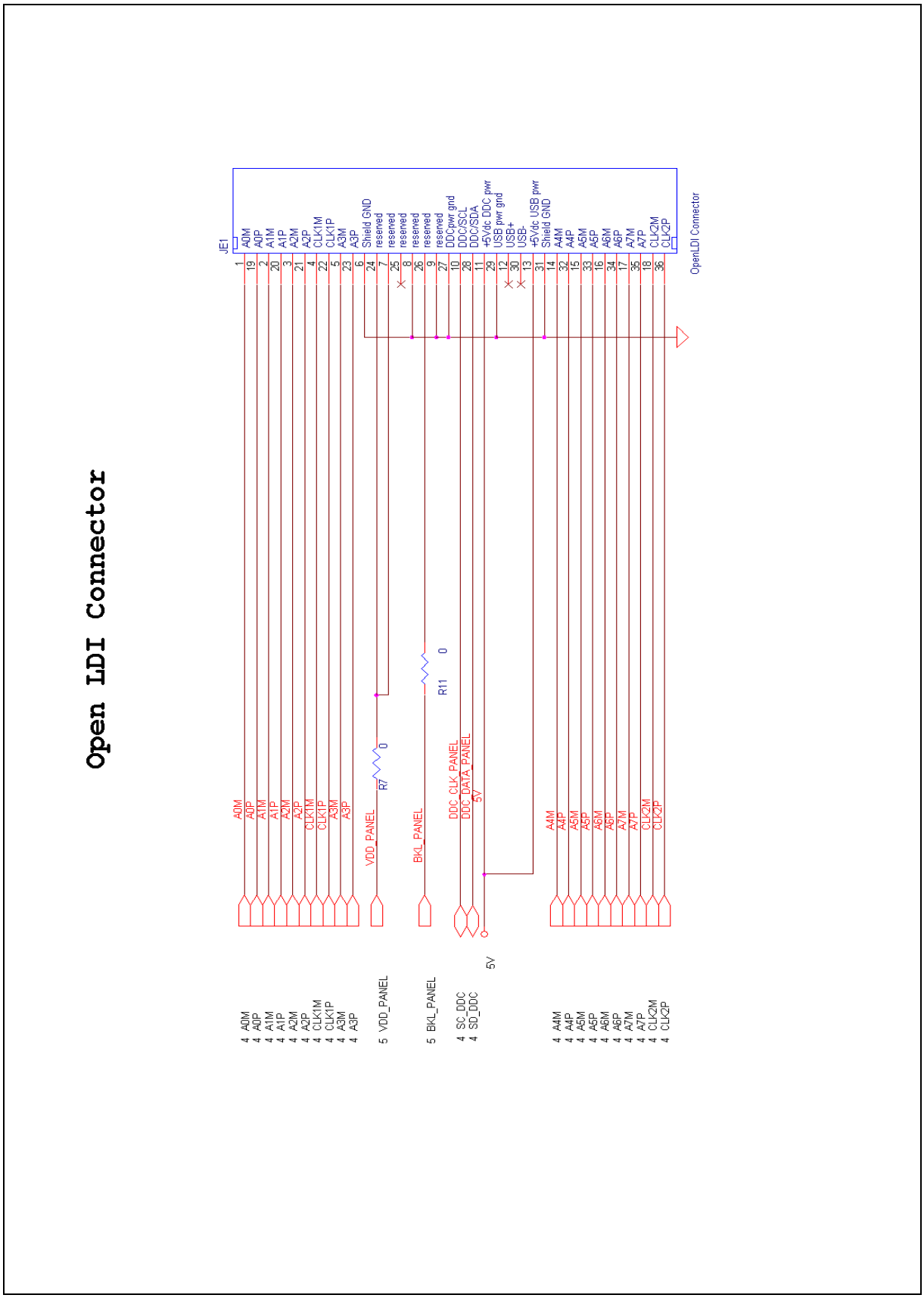
"ellipse"




Chrontel
CH7308
64 pin - LQFP


IMPORTANT:
The power to the LVDS panel backlight and the LVDS panel logic circuit are specific to the particular panel you are using. The current setup supplies the LVDS backlight with 12V and the LVDS logic circuit with 3.3V when the 3 pin jumper J7 and J8 are stuffed in the 1-2 position. For Voltages that require different voltages please supply the required voltage to EXVDD and EXBKL and stuff J7 and J8 to the 2-3 position. Please check with LVDS specification on the power requirements of your chosen panel.
BKL_PANEL 6
VDD_PANEL 6
EXBKL
EXVDD
12V
3.3V
ENAVDD
ENABKL
GND
External LVDS VDD Supply
External LVDS Backlight Supply
POWER CLIP

Open LDI Connector



3.2 Reference Design BOM

CH7308A Bill of Materials

Revision 1.0 December 22, 2004

Item	Qty	Reference	Part	Comments
1	1	CON1	x4 SDVO	
2	12	C2,C3,C7,C8,C9,C10,C11,	0.1uf	
		C16,C17,C18,C19,C20		
3	2	C4,C5	22P	
4	8	C6,C12,C15,C21,C22,C24,	10uf	
		C25,C27		
5	2	C13,C14	100nf	
6	1	C23	0.1U	
7	1	C26	0.33uf	
8	1	JE1	OpenLDI Connector	
9	4	J1,J2,J3,J4	JUMPER	
10	2	J7,J8	HEADER 3	
11	4	L1,L3,L4,L5	Bead	
12	3	PO1,PO2,PO3	GND	
13	3	Q1,Q2,Q3	2N7002	
14	1	R1	2.4k	
15	6	R2,R3,R5,R6,R15,R16	5.6k	
16	1	R4	0	
17	2	R7,R11	0	
18	1	R8	33	
19	2	R9,R10	10k	
20	1	R12	* 0	
21	2	R13,R14	4.7K	
22	2	R17,R18	3.6k	
23	6	TP1,TP2,TP3,TP4,TP5,TP6	TEST POINT	
24	1	U1	CH7308	
25	1	U2	24C16	
26	1	U4	G950T63U	
27	1	U5	SI4953	
28	1	U6	MC78L05	
29	1	Y1	14.31818MHz	

100-0000-127

4. Revision History

Revision	Date	Section	Description
1.0	12/22/04	All	First Revision.
1.1	8/8/05	Introduction	Note regarding the maximum pixel rate of the CH7308A rev. D added.
1.2	12/21/05	All	Added the CH7308B.
		Introduction	Added a table to include the maximum pixel rates for the CH7308 and a note mentioning that the HSWidth in the DTD must be set to an even value.
1.3	2/6/06	All, Introdution	Added information in the Introduction section stating that CH7308A and CH7308B are identical in connection. Replaced CH7308A/B with CH7308

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